DCSG S9500-22XST
CPLD Specification

Revision 1.0

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June 8, 2021

UfiSpace Technology Corporation

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Revision History

Date	Rev	Author	Summary of Change
Jun. 8, 2021	R0.1	Tom Chen	First Draft Release

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1 Overview

By providing 1GE, 10GE, 25GE and 100GE high speed Ethernet ports and IEEE 1588v2, SyncE timing synchronization features, S9500-22XST enables service providers to deliver next-generation technologies such as 5G mobile Ethernet network, which requires higher data bandwidth and more precise timing synchronization.

With temperature-hardened, high-throughput, small form factor, low-power-consumption & redundancy (PSU and FAN) features, S9500-22XST delivers high system reliability, Ethernet switching performance and intelligence to the network edge in a flexible 1U form factor that helps reduce infrastructure and administrative costs.

S9500-22XST I/O ports, PSU and FAN configurations are shown as below:

1G/10G/25G/100G Ethernet Ports	FAN	PSU	Synchronization
4 x 10/100/1000 Base-T 8 x 1G/10G SFP+ 8 x 1G/10G/25G SFP28 2 x 40G/100G QSFP28	2+1 Redundant 4028 FAN Tray	1+1 Redundant 200W slim PSU	GNSS, T1/E1, ToD, 1PPS, 10M In & Out

Table 1-1 S9500-22XST Configuration Information



Figure 1-1 S9500-22XST ID Rendering

2 High-Level Description

This section describes key features, system block diagram and system mechanical outline for S9500-22XST.

2.1 Feature Summary

- Ethernet I/O ports:
  - 4 x 10/100/1000 Base-T ports
  - 8 x 10GE SFP+ ports
  - 8 x 25GE SFP28 ports
  - 2 x 100GE QSFP28 ports
- Front/Real panel LED indicators:
  - 1 x Power status LED
  - 1 x FAN status LED
  - 1 x System status LED
  - 1 x Synchronization status LED
  - 1 x GNSS\GPS status LED
  - Per port FAN status LED
  - Per port PSU status LED
  - Per port link status LED
- Management interfaces:
  - 1 x GE OOB management port (CPU)
  - 1 x USB2.0 Type-A general purpose port
  - 1 x RS232 console port in RJ45 form factor
  - 1 x USB console port in Micro USB form factor
  - 1 x Tact switch for system reset/reload default configuration
- Timing Synchronization:
  - 1588v2 and SyncE with T-GM, T-TSC, T-TC, T-OC, T-BC support
  - Input source : GNSS/GPS, E1/T1, ToD, 1PPS and 10MHz
  - Output source : 1PPS and 10MHz

2.2 Component Summary

- PCBA:
  - 1 x Switch board
  - 1 x CPU card
  - 1 x FAN card
  - 1 x PSU card
  - 1 x LED card
- On board key components:
  - Switch Board

- 1 x MAC Qumran-AX BCM88470
- 4 x 512MB DDR4 SDRAM @ 1200MHz
- 1 x Quad port 1GbE PHY BCM54140
- 1 x Management CPLD 10M04SAU169I7G
- 1 x PCIe/NCSI NIC I210-IT for CPU & BMC
- 1 x SyncE & IEEE 1588 DPLL 82P33831
- 1 x Clock jitter attenuator buffer Si5344D
- 1 x GNSS/GPS module NEO-M8T
- 1 x T1/E1 transceiver 82P2281

■ CPU Card

- 1 x CPU Broadwell-DE D-1519 with quad core @ 1.5GHz
- 1 x 8GB DDR4 SODIMM memory module with ECC support
- 1 x 32GB SATA3 M.2 SSD Memory module

● PSU& FAN:

- 2x 200W slim PSUs with redundancy support
- 3x 4028 FAN tray modules with redundancy support

3 CPU Card

CPU card CPLD can be accessed through LPC with based address 0x600.

CPU CPLD resistor mapping is shown as below:

Offset	Register Name	Function/Notes
0x00	CPLD Revision	CPLD revision register
0x01	Status-0	Status register for reading input signals from BMC
0x02	Status-1	Status register for reading information of BIOS flash selection
0x03	Cntrl-0	Control register used to send signals to BMC
0x04	Cntrl-1	Control register used to send signals to BMC
0x05	Mask-0	
0x06	SKU ID	SKU ID register

CPU CPLD resistor description is shown as below:

CPLD Revision				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x00	D[3:0]	1011	RO	CPLD Revision Number, hardwired
	D[7:4]	0000	RO	CPLD Revision Number, hardwired

Status-0				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x01	D[0]	x	RO	Reserved
	D[1]	x	RO	Reserved
	D[2]	x	RO	Reserved
	D[3]	x	RO	Reserved
	D[4]	x	RO	Reserved
	D[5]	x	RO	Reserved
	D[6]	1	RW	BMC_to_HOST_INT_L Non-maskable Interrupt Request from BMC
	D[7]	1	RW	BMC_to_HOST_NMI_L Interrupt Request from BMC

Mask-0				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x05	D[0]	1	RW	PCIE_RESET_MASK Mask to disable CPLD_PCIE_RESET_N going to motherboard.
	D[1]	x	RW	Reserved

	D[2]	x	RW	Reserved
	D[3]	x	RW	Reserved
	D[4]	x	RW	Reserved
	D[5]	x	RW	Reserved
	D[6]	1	RW	BMC_to_HOST_INT_Mask Mask to disable BMC-to-Host Interrupt.
	D[7]	x	RW	Reserved

Cntrl-0				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x03	D[0]	x	RW	Reserved
	D[1]	x	RW	Reserved
	D[2]	x	RW	Reserved
	D[3]	x	RW	Reserved
	D[4]	1	RW	HOST_to_BMC_INT_L Interrupt Request to BMC
	D[5]	1	RW	HOST_to_BMC_RST_L Reset signal to reset BMC from CPU
	D[6]	1	RW	Reserved
	D[7]	1	RW	HOST_to_MB_RST_L Reset signal to reset motherboard from CPU

Cntrl-1				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x04	D[0]	1	RW	WDT_RCVRY_EN This bit enables the watchdog recovery logic. It controls BIOS_MUX_SEL
	D[1]	1	RW	WDT_DOG_EN This bit enables the Watchdog timer during boot process. The CPU must disable this bit right after it boots. It is enabled upon power up or SYS_RS_L
	D[2]	x	RW	Reserved
	D[3]	x	RW	Reserved
	D[4]	x	RW	Reserved
	D[5]	x	RW	Reserved
	D[6]	x	RW	Reserved
	D[7]	0	RW	BIOS_MUX_SEL This bit is not reset with a hardware reset. It will default to its value when power up, only. This value is used to write to the BIOS MUX selector when watchdog recovery is disabled (WDT_RCVRY_EN=0).

Status-1				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x02	D[0]	x	RO	Reserved
	D[1]	x	RO	Reserved
	D[2]	x	RO	Reserved
	D[3]	x	RO	Reserved
	D[4]	x	RO	Reserved
	D[5]	x	RO	Reserved
	D[6]	x	RO	Reserved
	D[7]	x	RO	BIOS_MUXSEL Actual value of BIOS_MUXSEL. If the CPLD watchdog logic triggered, it will be different than this bit. Otherwise, it will be same value.

SKU ID				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x06	D[0]	1	RO	Build ID [1:0] = 01
	D[1]	0	RO	00 : 1 01 : 2 10 : 3 11 : 4
	D[2]	1	RO	HW_REV_ID[1..0]=11
	D[3]	1	RO	Hardware Revision [1:0]= 10 00: Proto 01: Alpha 10: Beta 11: PVT
	D[4]	0	RO	SKU_ID[3..0]
	D[5]	0	RO	0000 : Apache BroadWell-DE CPU board
	D[6]	0	RO	0001 : Reserved
	D[7]	0	RO	: 1111 : Reserved

4 Main Board

4.1 Features Summary and Diagram

Main functional blocks in the system CPLD include the following:

- Component reset control and interrupt management
- Register map for PSU / FAN status and interrupt
- Register map for fiber port status and interrupt
- System & FAN status LED control

Two interfaces connected between CPU and CPLD: I2C bus and LPC bus, BMC share the same I2C interface with CPU, it's done by an I2C mux. I2C bus for CPU access is for CPLD firmware upgrade only. CPU/BMC can access CPLD by I2C bus channel 0 and address is 7b'0110011x (0x33). LPC interface will be active to access CPLD with LPC address 0x7xx.

CPLD function diagram is shown as below:

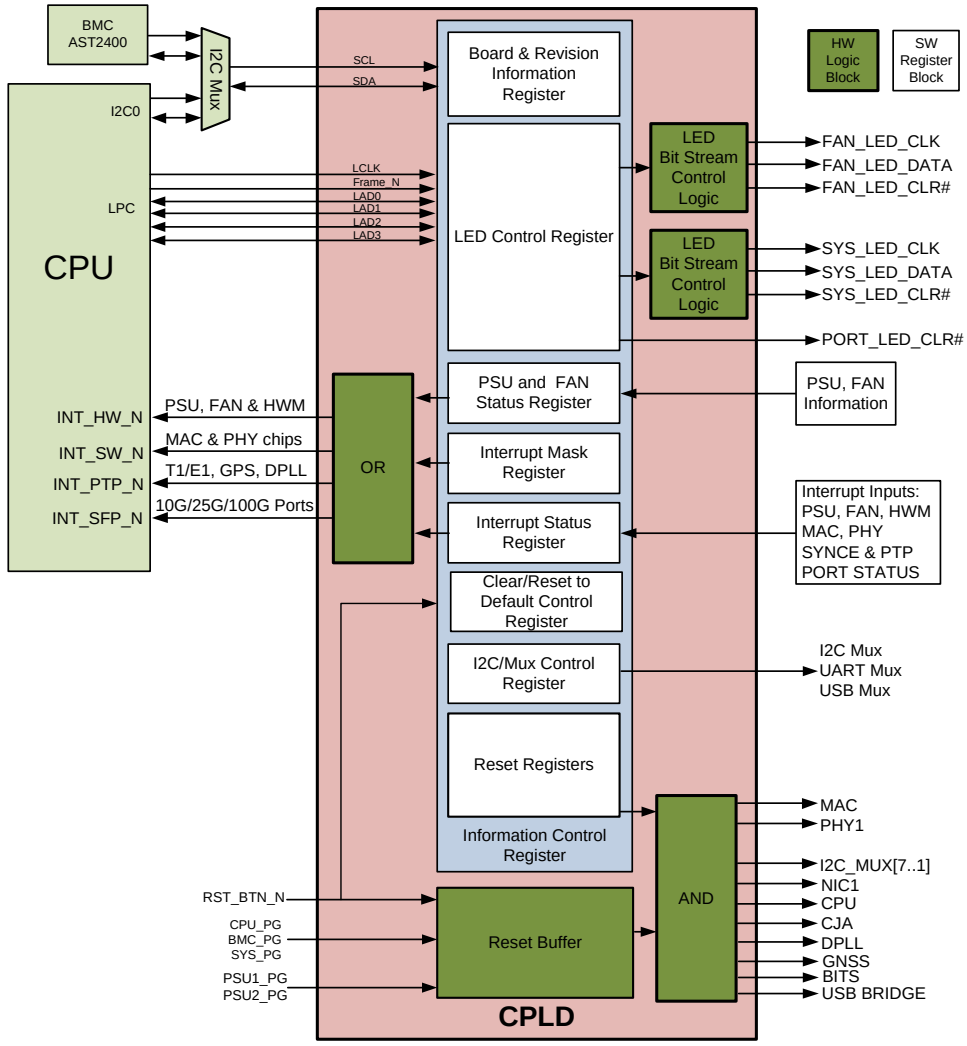


Figure 4-1 CPLD diagram

4.2 MB CPLD Pin Assignment

Switch board CPLD pin assignment is shown as below:

Pin Number	Pin Type	Pin Name	Net Name	Function Description
D1	IO	IO_1_1	LPC_LAD1_PCH	LPC_LAD1 to/from CPLD
C1	IO	IO_1_2	LPC_LAD3_PCH	LPC_LAD3 to/from CPLD
C2	IO	IO_1_3	LPC_FRAME_PCH_N	LPC frame signal to CPLD
B1	IO	IO_1_4	GNSS_ANT_SHORT_N	GNSS Module antenna short indication
E3	IO	IO_1_5	LPC_LAD2_PCH	LPC_LAD2 to/from CPLD
F1	IO	IO_1_6	INT1_GNSS_N	GNSS module interrupt output to CPLD
E4	IO	IO_1_7	PWROK_SYS_DC	System DC Power ok to CPLD
E1	IO	IO_1_8	LPC_LAD0_PCH	LPC_LAD0 to/from CPLD
H1	IO	IO_1_9	UART_CPU_BMC_MUX_SEL	UART host select control by CPLD
F4	IO	IO_1_10	RST_SW_BTN_N	System Reset Button signal to CPLD
G4	IO	IO_1_11	BMC_HEATER_DIS_N	BMC heater enable indication
H2	IO	IO_1_12	LED_SYS_STAT_SCLK	System status led serial clock signal
H3	IO	IO_1_13	RST_GNSS_N	GNSS Module reset control by CPLD
J1	IO	IO_2_1	LED_INIT_CLR_N	ETH_STAT/SYS_STAT/FAN STAT LED clear signal control by CPLD
H6	IO	IO_2_2	INT_PTP_CPLD_TO_CPU_N	PTP interrupt singal to CPU
J2	IO	IO_2_3	LED_SYS_STAT_SDAT	System status led serial data signal
H5	IO	IO_2_4	CLK_33M_LPC_CPLD	CPLD LPC clock source
M1	IO	IO_2_5	RST_CPU_TO_MB_PCIE_N	PCIE reset signal to CPLD
H4	IO	IO_2_6	RST_CPLD_TO_CPU_N	CPU Card reset control by CPLD
M2	IO	IO_2_7	LED_CPLD_STATUS1	CPLD Status LED1 control by CPLD
N2	IO	IO_2_8	RST_BMC_PCIE_N	Reserved
L1	IO	IO_2_9	RST_BMC_WDT_L	Reserved
N3	IO	IO_2_10	USB_PWR_EN	USB Port Power enable by CPLD
L2	IO	IO_2_11	INT_CPLD_NMI_N	CPLD non mask interrupt signal to CPU/BMC
M3	IO	IO_2_12	USB_PWR_OC_N	USB Port over current interrupt to CPLD
K1	IO	IO_2_13	RST_BMC_DDR3_CPLD_N --> ~~25M_JA_CLKSEL~~ JA_25M_CLKSEL	25M JA_5P49V6965A202NLGI8 input clock source select control by CPLD
L3	IO	IO_2_14	SMU_DPLL1_LOCK	DPLL 82P33831 DPLL1 Lock interrupt to CPLD
K2	IO	IO_2_15	BMC_PWRGD_CPLD	BMC power good indication
L5	IO	IO_3_1	~~SFP+_PWR_OC_GP1~~ --> PHY1_SYNCE_RCVD_LOCK1	BCM54140 1G PHY SYNCE Recovery clock lock2
M4	IO	IO_3_2	LED_CPLD_STATUS2	CPLD Status LED2 control by CPLD
L4	IO	IO_3_3	INT_PSU2_N	PSU2 Module interrupt to CPLD
M5	IO	IO_3_4	RST_NIC1_PCIE_N	NIC1 I210 PCIE reset control by CPLD
K5	IO	IO_3_5	RST_I2C_MUX2_N	I2C MUX2 reset control by CPLD
N4	IO	IO_3_6	RST_NIC1_N	NIC1 I210 system reset control by CPLD
J5	IO	IO_3_7	INT_SFP+_FLT_N0	Optical module TX FLT interrupt to CPLD
N5	IO	IO_3_8	RST_PHY1_N	PHY1 BCM82780F reset control by CPLD
N6	IO	IO_3_9	RST_I2C_MUX3_N	I2C MUX3 reset control by CPLD
N7	IO	IO_3_10	RST_I2C_MUX4_N	I2C MUX4 reset control by CPLD
M7	IO	IO_3_11	INT_SFP+_ABS_N0	Optical module presence to CPLD
N8	IO	IO_3_12	SMU_DPLL2_LOCK	DPLL 82P33831 DPLL2 Lock interrupt to CPLD
J6	IO	IO_3_13	INT_CHIP_CPLD_TO_CPU_N	Chip interrupt signal to CPLD
M8	IO	IO_3_14	RST_BMC_LPC_N	BMC LPC reset control by CPLD
K6	IO	IO_3_15	INT_SFP+_LOS_N0	Optical module RX loss interrupt to CPLD
M9	IO	IO_3_16	RST_I2C_MUX5_N	I2C MUX5 reset control by CPLD
J7	IO	IO_3_17	INT_FAN_CARD_N	Fan Card interrupt to CPLD
N11	IO	IO_3_18	RST_I2C_MUX6_N	I2C MUX6 reset control by CPLD
K7	IO	IO_3_19	RST_CPU_PLTRST_N	CPU PLTRST signal to CPLD
N12	IO	IO_3_20	INT_QSFP28_N	QSFP28 Module interrupt to CPLD
M13	IO	IO_3_21	~~SFP+_PWR_OC_GP3~~ -> PHY1_SYNCE_RCVD_LOCK2	BCM54140 1G PHY SYNCE Recovery clock lock2
N10	IO	IO_3_22	INT_SFP+_FLT_N1	Optical module TX FLT interrupt to CPLD
M12	IO	IO_3_23	RST_I2C_MUX1_N	I2C MUX1 reset control by CPLD
N9	IO	IO_3_24	SFP+_PWR_OC_GP2	Optical Module over current interrupt to CPLD
M11	IO	IO_3_25	INT_SFP+_ABS_N1	Optical module presence to CPLD
L11	IO	IO_3_26	I2C_CPLD_SCL	CPLD I2C bus clock signal
J8	IO	IO_3_27	CPU_PRSNT_L	CPU Card presence to CPLD
K8	IO	IO_3_28	CPU_TO_CPLD_PWRGD	CPU Power Good indication
M10	IO	IO_3_29	INT_SFP+_LOS_N1	Optical module RX loss interrupt to CPLD

L10	IO	IO_3_30	INT_SMU_N	DPLL 82P33831 interrupt to CPLD
K10	IO	IO_5_1	I2C0_HWM_MUX_SEL	HWM I2C Host select control by CPLD
K11	IO	IO_5_2	I2C_CPLD_SDA	CPLD I2C bus data signal
J10	IO	IO_5_3	INT_HWM_NMI_N	HWM non maskable interrupt to CPLD
L12	IO	IO_5_4	SFP28_PWR_OC_N	SFP28 Module over current interrupt to CPLD
K12	IO	IO_5_5	MAC_MCUPLL_LOCK	MAC MCUPLL Lock signal to CPLD
L13	IO	IO_5_6	RST_I2C_MUX7_N	I2C MUX7 reset control by CPLD
J12	IO	IO_5_7	RST_BITS_N	BITS reset control by CPLD
K13	IO	IO_5_8	RST_USB_BRIDGE_N	USB Bridge reset control by CPLD
J9	IO	IO_5_9	RST_CJA_N	CJA_Si5344D-D09606-GMR Reset control by CPLD
J13	IO	IO_5_10	INT_BITS_N	BITS interrupt output to CPLD
H10	IO	IO_5_11	QSFP28_PWR_OC_N	QSFP28 Module over current interrupt to CPLD
H13	IO	IO_5_12	RST_SMU_N	DPLL 82P33831 reset control by CPLD
H9	IO	IO_5_13	INT_CJA_LOL_N	CJA_Si5344D lose of lock to CPLD
G13	IO	IO_5_14	PWR_OFF_MAC	MAC power off control by CPLD
H8	IO	IO_5_15	INT_PHY3_N	PHY3 BCM82391 interrupt output to CPLD
G12	IO	IO_5_16	MAC_COREPLL_LOCK	MAC COREPLL LOCK signal to CPLD
G9	IO	IO_6_1	INT_MAC_N	MAC interrupt output to CPLD
G10	IO	IO_6_2	INT_CJA_INTR_N	CJA_Si5344D interrupt to CPLD
F13	IO	IO_6_3	PTP_1PPS_MUX_SEL -> ~~25M_JA_SEL1~~ JA_25M_SEL1	25M JA_5P49V6965A202NLGI8 Config bit 1 control by CPLD
E13	IO	IO_6_4	INT_FAN3_N	Fan1 Module interrupt to CPLD
F12	IO	IO_6_5	INT_FAN4_N	Fan2 Module interrupt to CPLD
E12	IO	IO_6_6	INT_FAN5_N	Resweved Fan Module interrupt to CPLD
F9		IO_6_7	RST_CPU_PWRBTN_N	CPU Card reset control by CPLD
D13	IO	IO_6_8	INT_FAN2_N	Fan0 Module interrupt to CPLD
F10	IO	IO_6_9	RST_MAC_N	MAC Reset Control by CPLD
C13	IO	IO_6_10	INT_FAN1_N	Reserved Fan Module interrupt to CPLD
F8	IO	IO_6_11	INT_TSEN_ALRT_N	Thermal sensor alert interrupt signal to CPLD
B12	IO	IO_6_12	LED_FAN_SDAT	Fan module status led serial data signal
E9	IO	IO_6_13	INT_TSEN_NMI_N	Thermal sensor non mask interrupt signal to CPLD
B11	IO	IO_6_14	FAN2_PRSNT_N	FAN0 Module presence to CPLD
C12	IO	IO_6_15	I2C_CPLD_ALRT_N	CPLD i2c alert output to CPU/BMC
B13	IO	IO_6_16	FAN3_PRSNT_N	FAN1 Module presence to CPLD
C11	IO	IO_6_17	FAN1_PRSNT_N	Reserved FAN Module presence to CPLD
A12	IO	IO_6_18	LED_FAN_SCLK	Fan module status led serial clock signal
E10	IO	IO_6_19	GNSS_ANT_ON	GNSS module antenna power on control
D9	IO	IO_6_20	RST_PHY3_N	PHY3 BCM82391 reset control by CPLD
D12	IO	IO_6_21	RST_I2C_MUX0_N	I2C MUX0 reset control by CPLD
D11	IO	IO_6_22	FAN45_TACH_SW	HWM_FAN2_TACH_IN input select control by CPLD
C10	IO	IO_8_1	PTP_TOD_RS422_TXD_EN	PTP ToD output enable control by CPLD
A8	IO	IO_8_2	PTP_1PPS_RS422_TXD_EN	PTP 1PPS output enable control by CPLD
C9	IO	IO_8_3	PTP_TOD_RS422_RXD_EN_N	PTP ToD intput enable control by CPLD
A9	IO	IO_8_4	PWREN_BMC_HEATER_CPLD	PWREN_BMC_HEATER_CPLD signal to CPLD
B10	IO	IO_8_5	PTP_1PPS_RS422_RXD_EN_N	PTP 1PPS intput enable control by CPLD
A10	IO	IO_8_6	FAN4_PRSNT_N	FAN2 Module presence to CPLD
B9	IO	IO_8_7	SMU_INPUT1_LOS_N	DPLL 82P33831 input source 1 loss interrupt to CPLD
A11	IO	IO_8_8	FAN5_PRSNT_N	Reserved FAN Module presence to CPLD
D8	IO	IO_8_9	PSU2_PRSNT_N	PSU2 Module Power good to CPLD
E8	IO	IO_8_10	RST_CPLD_TO_BMC_SYS_L -> ~~25M_JA_SEL0~~ JA_25M_SEL0	25M JA_5P49V6965A202NLGI8 Config bit 0 control by CPLD
B7	IO	IO_8_11	PSU2_PWROK	PSU2 Module presence to CPLD
D7	IO	IO_8_12	CPLD_CONFIG_SEL	CPLD config select
A7	IO	IO_8_13	GNSS_ANT_PWREN	GNSS Module antenna Power enable indication
A6	IO	IO_8_14	I2C_CPLD_MUX_EN	I2C_CPLD MUX Enable control
B6	IO	IO_8_15	I2C0_MGMT_MUX_SEL	MGMT I2C Host select control by CPLD
A4	IO	IO_8_16	INT_LOAD_DEFAULT_N	Load deault interrupt signal to CPU/BMC
B5	IO	IO_8_17	INT_SFP_CPLD_TO_CPU_N	Optical Module interrupt signa sentl to CPU
A3	IO	IO_8_18	INT_PSU1_N	PSU1 Module interrupt to CPLD
E6	IO	IO_8_19	INT_PHY1_N	PHY1 BCM82780F interrupt output to CPLD
B3	IO	IO_8_20	PSU1_PWROK	PSU1 Module Power good to CPLD
B4	IO	IO_8_21	BMC_HEATING_DONE	BMC heater heating done indication
A5	IO	IO_8_22	SMU_DPLL3_LOCK	DPLL 82P33831 DPLL3 Lock interrupt to CPLD
A2	IO	IO_8_23	PSU1_PRSNT_N	PSU1 Module presence to CPLD
B2	IO	IO_8_24	GNSS_ANT_OPEN	GNSS Module antenna open indication
N13	GND	GND_1	GND	Ground

N1	GND	GND_2	GND	Ground
M6	GND	GND_3	GND	Ground
L9	GND	GND_4	GND	Ground
J4	GND	GND_5	GND	Ground
H12	GND	GND_6	GND	Ground
G7	GND	GND_7	GND	Ground
F3	GND	GND_8	GND	Ground
E11	GND	GND_9	GND	Ground
F2	VCCIO_1	VCCIO_1_1	P3V3	VCCIO_1 Power
G3	VCCIO_1	VCCIO_1_2	P3V3	VCCIO_1 Power
K3	VCCIO_2	VCCIO_2_1	P3V3	VCCIO_2 Power
J3	VCCIO_2	VCCIO_2_2	P3V3	VCCIO_2 Power
G1	IO	TMS	JTAG_CPLD_TMS	CPLD Jtag TMS signal
F5	IO	TDI	JTAG_CPLD_TDI	CPLD Jtag TDI signal
G2	IO	TCK	JTAG_CPLD_TCK	CPLD Jtag TCK signal
F6	IO	TDO	JTAG_CPLD_TDO	CPLD Jtag TDO signal
E5	IO	JTAGEN	JTAG_CPLD_EN	CPLD Jtag enable signal
E7	input only	nCONFIG	CPLD_CONFIG_EN	CPLD config enable
D6	IO	CRC_ERROR	CPLD_CRC_ERROR	CPLD CRC error output
C4	IO	nSTATUS	CPLD_STATUS_N	CPLD Status output
C5	IO	CONF_DONE	CPLD_CONF_DONE	CPLD Configure done signal output
D5	GND	GND_10	GND	Ground
C3	GND	GND_11	GND	Ground
B8	GND	GND_12	GND	Ground
A13	GND	GND_13	GND	Ground
A1	GND	GND_14	GND	Ground
L8	VCCIO_3	VCCIO_3_1	P3V3	VCCIO_3 P3V3 Power
L7	VCCIO_3	VCCIO_3_2	P3V3	VCCIO_3 P3V3 Power
L6	VCCIO_3	VCCIO_3_3	P3V3	VCCIO_3 P3V3 Power
J11	VCCIO_5	VCCIO_5_1	P3V3	VCCIO_5 P3V3 Power
H11	VCCIO_5	VCCIO_5_2	P3V3	VCCIO_5 P3V3 Power
G11	VCCIO_6	VCCIO_6_1	P3V3	VCCIO_6 P3V3 Power
F11	VCCIO_6	VCCIO_6_2	P3V3	VCCIO_6 P3V3 Power
C8	VCCIO_8	VCCIO_8_1	P3V3	VCCIO_8 P3V3 Power
C7	VCCIO_8	VCCIO_8_2	P3V3	VCCIO_8 P3V3 Power
C6	VCCIO_8	VCCIO_8_3	P3V3	VCCIO_8 P3V3 Power
E2	NC	NC_1	N84802297	NC
D3	NC	NC_2	P2V5_VREF	NC
D2	NC	NC_3	N84802108	NC
K4	VDDA	VDDA_1	VFLT_P3V3_CPLD_VDDA	Power
D10	VDDA	VDDA_2	VFLT_P3V3_CPLD_VDDA	Power
D4	VDDA	VDDA_3	VFLT_P3V3_CPLD_VDDA	Power
K9	VDDA	VDDA_4	VFLT_P3V3_CPLD_VDDA	Power
H7	VCC_ONE	VCC_ONE_1	P3V3	P3V3 Power
G8	VCC_ONE	VCC_ONE_2	P3V3	P3V3 Power
G6	VCC_ONE	VCC_ONE_3	P3V3	P3V3 Power
F7	VCC_ONE	VCC_ONE_4	P3V3	P3V3 Power
G5	Clock	CLK0_n	CLK_25M_CPLD_CLK0	CPLD core clock source

4.3 MB CPLD Register Mapping

Switch board CPLD can be accessed through LPC with based address 0x700.

Offset	Default Value	Register Name	Function
0x00	**0x08**	Board ID	Reserved
0x01	**0x00**	Extend Board ID	Reserved
0x02	0x00	Code Version	CPLD firmware version
0x03	0xFF	PLL Lock	DPLL & MAC lock status
0x04	0xFF	DPLL Input Lost	IDT DPLL input loss control
0x05	**0xF1**	Fan Present	FAN presence status
0x06	0xC4	Multiple Interface Select	UART, I2C and 1PPS mux control
0x07	0x00	PTP Control	ToD port 1PPS & ToD input/output control
0x08	0x37	Power Status	PSU, BMC, MB, CPU power status
0x09	0xE8	Power Control	USB and heater power control
0x0A	0x3F	Port Over Current	SFP and USB ports over current interrupt
0x0B	0x1F	Fan Interrupt	Fan status(stop or working) interrupt
0x0C	0x1F	NMI Interrupt	Hardware(Thermal sensor, PSU, HWM, Heater) NMI interrupt
0x0D	0x07	MAC & PHY Interrupt	MAC & 10G, 100G PHY interrupt
0x0E	0x4F	SyncE & PTP Interrupt	DPLL, JA, GNSS, BITS interrupt
0x0F	0x7F	SFP Port Interrupt	SFP port transceivers interrupt
0x10	0x1F	Miscellaneous Interrupt	Miscellaneous interrupt
0x11	0x00	Interrupt Mask	Interrupt to CPLD mask
0x12	0x87	Reset Status	CPU and reset button status
0x13	0xFF	I2C Mux Reset	I2C mux reset control
0x14	0x1F	BMC Reset	BMC reset control
0x15	0x07	MAC & PHY Reset	MAC, 10G, 100G PHY reset control
0x16	0xFF	Miscellaneous Reset	DPLL, JA, BITS, GNSS, HWM and NIC reset control
0x17	0x01	Global Reset	Global reset control
0x18	0x00	System LED Control1	Front panel LED control
0x19	0x00	System LED Control2	Front panel LED control
0x1A	0x00	System LED Blinking	Front panel LED blinking rate control
0x1B	**0x02**	Fan4 & Fan5 TACH Switch	Fan2 TACH to HWM control
0x1C	0x01	GNSS Status	GNSS status
0x1D	0xFF	Interrupt Debug Registor	Debug for interrupt signal trigger
0x1E	**0x10**	TSPLL Clock Source Control	TSPLL Clock Source Control

4.4 MB CPLD Register Description

Board ID				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x00	D[1:0]	00	RO	Build REV [1:0] 00: 0 01: 1 10: 2 11: 3
	D[3:2]	10	RO	HW REV[1:0] 00: Proto 01: Alpha 10: Beta 11: PVT
	D[7:4]	0000	RO	Model ID [3:0] 0000: S9500_22XST

Extend Board ID				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x01	D[3:0]	0000	RO	Board ID [3:0] Reserved
	D[7:4]	0000	RO	Reserved

CPLD Version				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x02	D[7:0]	00000000	RO	CPLD code Revision Bit[7:0]: 00000000: CPLD Code Revision is X.00 00000001: CPLD Code Revision is X.01 00000010: CPLD Code Revision is X.02 00000011: CPLD Code Revision is X.03 …

Clock and Timing Status				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x03	D[0]	1	RO	SMU_DPLL1_LOCK 0：82P33831 DPLL1 is not locked 1：82P33831 DPLL1 is locked
	D[1]	1	RO	SMU_DPLL2_LOCK 0：82P33831 DPLL2 is not locked 1：82P33831 DPLL2 is locked

Clock and Timing Status				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
	D[2]	1	RO	SMU_DPLL3_LOCK 0：82P33831 DPLL3 is not locked 1：82P33831 DPLL3 is locked
	D[3]	1	RO	Reserved
	D[4]	1	RO	MAC_COREPLL_LOCK 0：MAC COREPLL is not lock 1：MAC COREPLL is lock
	D[5]	1	RO	MAC_MCUPLL_LOCK 0：MAC MCUPLL is not lock 1：MAC MCUPLL is lock
	D[6]	1	RO	PHY1_SYNCE_RCVD_LOCK1 0：PHY1 SYNCE REC_CLK[1] is not lock 1：PHY1 SYNCE REC_CLK[1] is lock
	D[7]	1	RO	PHY1_SYNCE_RCVD_LOCK2 0：PHY1 SYNCE REC_CLK[2] is not lock 1：PHY1 SYNCE REC_CLK[2] is lock

DPLL Input Lost				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x04	D[0]	1	RW	Reserved
	D[1]	1	RW	SMU_INPUT1_LOS_N 0：82P33831 input x lost assert 1：82P33831 input x lost de-assert
	D[2]	1	RW	Reserved
	D[3]	1	RW	Reserved
	D[4]	1	RW	Reserved
	D[5]	1	RW	Reserved
	D[6]	1	RW	Reserved
	D[7]	1	RW	Reserved

Fan Present				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x05	D[0]	1	RO	Reserved
	D[1]	0	RO	FAN0_PRSNT_N 0：Fan0 present 1：Fan0 absent
	D[2]	0	RO	FAN1_PRSNT_N 0：Fan1 present 1：Fan1 absent
	D[3]	0	RO	FAN2_PRSNT_N 0：Fan2 present 1：Fan2 absent

Fan Present				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
	D[4]	1	RO	Reserved
	D[5]	1	RO	Reserved
	D[6]	1	RO	Reserved
	D[7]	1	RO	Reserved

Multiple Interface Select				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x06	D[0]	0	RW	Reserved
	D[1]	0	RW	UART_CPU_BMC_MUX_SEL 0：UART console port connect to CPU 1：UART console port connect to BMC
	D[2]	0	RW	Reserved
	D[3]	0	RW	I2C0_MGMT_MUX_ SEL 0：BMC I2C2 control MGMT I2C device(BMC I2C2 connect to MGMT I2C) 1：CPU I2C0 control MGMT I2C device(CPU I2C0 connect to MGMT I2C)
	D[4]	0	RW	Reserve
	D[5]	0	RW	I2C0_HWM_MUX_SEL 0：Hardware monitor I2C connect to BMC I2C1 1：Hardware monitor I2C connect to CPU I2C0
	D[6]	0	RW	Reserved
	D[7]	0	RW	Reserved

PTP Control				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x07	D[0]	0	RW	PTP_TOD_RS422_TXD_EN 0：Disable ToD port UART TX 1：Enable ToD port UART TX
	D[1]	0	RW	PTP_TOD_RS422_RXD_EN_N 0：Enable ToD port UART RX 1：Disable ToD port UART RX
	D[2]	0	RW	PTP_1PPS_RS422_TXD_EN 0：Disable ToD 1PPS TX 1：Enable ToD 1PPS TX
	D[3]	0	RW	PTP_1PPS_RS422_RXD_EN_N 0：Enable ToD 1PPS RX 1：Disable ToD 1PPS RX
	D[4]	0	RW	Reserve

PTP Control				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
	D[5]	0	RW	Reserve
	D[6]	0	RW	Reserve
	D[7]	0	RW	Reserve

Power Status				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x08	D[0]	1	RO	PWROK_SYS_DC 0：Switching subsystem power is abnormal 1：Switching subsystem power is ok
	D[1]	1	RO	CPU_TO_CPLD_PWRGD 0：CPU power is not ready 1：CPU power is ok
	D[2]	1	RO	BMC_PWRGD 0：BMC power is not ready 1：BMC power is ok
	D[3]	0	RO	CPU_PRSNT_L 0：CPU is present 1：CPU is absent
	D[4]	1	RO	PSU1_PWROK 0：PSU1 Power is abnormal. 1：PSU1 Power is OK.
	D[5]	1	RO	PSU2_PWROK 0：PSU2 Power is abnormal. 1：PSU2 Power is OK.
	D[6]	0	RO	PSU1_PRSNT_N 0：PSU1 Present 1：PUS1 Absent
	D[7]	0	RO	PSU2_PRSNT_N 0：PSU2 Present 1：PUS2 Absent

Power Control				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x09	D[0]	0	RW	PWR_OFF_MAC 0：MAC power is normal 1：Turn off MAC power
	D[1]	0	RW	Reserved
	D[2]	0	RW	Reserved

Power Control				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
	D[3]	1	RW	USB_PWR_EN 0：USB power is disabled 1：USB power is enabled
	D[4]	0	RW	BMC heater power enable 0：Normal 1：Force BMC heater power enabled
	D[5]	1	RW	Reserve
	D[6]	1	RW	Reserve
	D[7]	1	RW	Reserve

Port Over Current				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x0A	D[0]	1	RO	Reserve
	D[1]	1	RO	SFP+_PWR_OC_GP2 1：Normal 0：SFP+ port 8~15 over current
	D[2]	1	RO	Reserve
	D[3]	1	RO	QSFP28_PWR_OC_N 1：Normal 0：QSFP28 port 0~1 over current
	D[4]	1	RO	SFP28_PWR_OC_N 1：Normal 0：SFP28 port 21~27over current
	D[5]	1	RO	USB_PWR_OC_N 1：Normal 0：USB port over current
	D[6]	0	RO	Reserve
	D[7]	0	RO	Reserve

Fan Interrupt				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x0B	D[0]	1	RO	Reserved
	D[1]	1	RO	INT_FAN0_N 0：Fan0 interrupt assert 1：Fan0 interrupt de-assert
	D[2]	1	RO	INT_FAN1_N 0：Fan1 interrupt assert 1：Fan1 interrupt de-assert

Fan Interrupt				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
	D[3]	1	RO	INT_FAN2_N 0：Fan2 interrupt assert 1：Fan2 interrupt de-assert
	D[4]	1	RO	Reserved
	D[5]	0	RO	Reserved
	D[6]	0	RO	Reserved
	D[7]	0	RO	Reserved

NMI Interrupt				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x0C	D[0]	1	RO	INT_FAN_CARD_N 0：Fan card interrupt assert 1：Fan card interrupt de-assert
	D[1]	1	RO	INT_HWM_NMI_N 0：Hardware monitor interrupt assert 1：Hardware monitor interrupt de-assert
	D[2]	1	RO	INT_PSU1_N 0：PSU1 interrupt assert 1：PSU1 interrupt de-assert
	D[3]	1	RO	INT_PSU2_N 0：PSU2 interrupt assert 1：PSU2 interrupt de-assert
	D[4]	1	RO	BMC_HEATING_DONE 0：BMC heater interrupt assert (BMC heater time out) 1：BMC heater interrupt de-assert
	D[5]	0	RO	Reserved
	D[6]	0	RO	Reserved
	D[7]	0	RO	Reserved

MAC & PHY Interrupt				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x0D	D[0]	1	RO	INT_MAC_N 0：MAC interrupt assert 1：MAC interrupt de-assert
	D[1]	1	RO	INT_PHY1_N 0：PHY1 interrupt assert 1：PHY1 interrupt de-assert
	D[2]	1	RO	Reserved
	D[3]	0	RO	Reserved
	D[4]	0	RO	Reserved

MAC & PHY Interrupt				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
	D[5]	0	RO	Reserved
	D[6]	0	RO	Reserved
	D[7]	0	RO	Reserved

SyncE & PTP Interrupt				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x0E	D[0]	1	RO	INT_CJA_INTR_N 0：Clock buffer Si5344D interrupt assert 1：Clock buffer Si5344D de-assert
	D[1]	1	RO	INT_CJA_LOL_N 0：Clock buffer Si5344D LOL interrupt assert 1：Clock buffer Si5344D LOL de-assert
	D[2]	1	RO	Reserved
	D[3]	1	RO	INT1_GNSS_N 0：GPS NEO-M8T-0 interrupt 1 assert 1：GPS NEO-M8T-0 interrupt 1 de-assert
	D[4]	1	RO	INT_BITS_N 0：BITS interrupt assert 1：BITS interrupt de-assert
	D[5]	1	RO	INT_SMU_N 0：DPLL interrupt assert 1：DPLL interrupt de-assert
	D[6]	0	RO	Reserved
	D[7]	0	RO	Reserved

SFP Port Interrupt				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x0F	D[0]	1	RO	INT_SFP+_FLT_N0 0：INT_SFP+_FLT_N0 interrupt assert 1：INT_SFP+_FLT_N0 interrupt de-assert
	D[1]	1	RO	INT_SFP+_FLT_N1 0：INT_SFP+_FLT_N1 interrupt assert 1：INT_SFP+_FLT_N1 interrupt de-assert
	D[2]	1	RO	INT_SFP+_LOS_N0 0：INT_SFP+_LOS_N0 interrupt assert 1：INT_SFP+_LOS_N0 interrupt de-assert
	D[3]	1	RO	INT_SFP+_LOS_N1 0：INT_SFP+_LOS_N1 interrupt assert 1：INT_SFP+_LOS_N1 interrupt de-assert

SFP Port Interrupt				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
	D[4]	1	RO	INT_SFP+_ABS_N0 0：INT_SFP+_ABS_N0 interrupt assert 1：INT_SFP+_ABS_N0 interrupt de-assert
	D[5]	1	RO	INT_SFP+_ABS_N1 0：INT_SFP+_ABS_N1 interrupt assert 1：INT_SFP+_ABS_N1 interrupt de-assert
	D[6]	1	RO	INT_QSFP28_N 0：INT_QSFP28_N interrupt assert 1：INT_QSFP28_N interrupt de-assert
	D[7]	0	RO	Reserved

Miscellaneous Interrupt				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x10	D[0]	1	RO	INT_TSEN_ALRT_N 0：Temperature sensor interrupt assert 1：Temperature sensor interrupt de-assert
	D[1]	1	RO	INT_TSEN_NMI_N 0：Temperature sensor NMI interrupt assert 1：Temperature sensor NMI interrupt de-assert
	D[2]	1	RO	Reserved
	D[3]	1	RO	Reserved
	D[4]	1	RO	INT_HWM_ALERT_N 0：Hardware monitor alert assert 1：Hardware monitor alert de-assert
	D[5]	0	RO	Reserved
	D[6]	0	RO	Reserved
	D[7]	0	RO	Reserved

Interrupt Mask				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x11	D[0]	1	RW	Global Mask 0：Normal 1：Mask all interrupts
	D[1]	0	RW	Fan Interrupt Mask 0：Normal 1：Mask fan0,fan1,fan2 interrupts

Interrupt Mask				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
	D[2]	0	RW	NMI Interrupt Mask 0：Normal 1：Mask NMI interrupts
	D[3]	0	RW	MAC & PHY Interrupt Mask 0：Normal 1：Mask MAC & PHY interrupts
	D[4]	0	RW	SyncE & PTP Interrupt Mask 0：Normal 1：Mask SyncE & PTP interrupts
	D[5]	0	RW	SFP Port Interrupt Mask 0：Normal 1：Mask SFP Port interrupts
	D[6]	0	RW	Miscellaneous Interrupt Mask 0：Normal 1：Mask Miscellaneous interrupts
	D[7]	0	RW	Reserve

Reset Status				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x12	D[0]	1	RO	RST_PLTRST_N 0：CPU platform reset assert 1：CPU platform reset de-assert
	D[1]	1	RO	RST_PCIE_CPU_TO_MB_N 0：PCIE CPU to main board reset assert 1：PCIE CPU to main board reset de-assert
	D[2]	1	RO	RST_SW_BTN_N 0：Switch Button reset assert 1：Switch Button reset de-assert
	D[3]	0	RO	Reserved
	D[4]	0	RO	Reserved
	D[5]	0	RO	Reserved
	D[6]	0	RO	Reserved
	D[7]	1	RO	RST_SW_BTN_N >5S (Load factory default) 0：Load system to factory default 1：No action

I2C Mux Reset				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x13	D[0]	1	RW	RST_I2C_MUX1_N 0：Reset I2C MUX1 1：Normal
	D[1]	1	RW	RST_I2C_MUX2_N 0：Reset I2C MUX2 1：Normal
	D[2]	1	RW	Reserved
	D[3]	1	RW	RST_I2C_MUX4_N 0：Reset I2C MUX4 1：Normal
	D[4]	1	RW	RST_I2C_MUX5_N 0：Reset I2C MUX5 1：Normal
	D[5]	1	RW	RST_I2C_MUX6_N 0：Reset I2C MUX6 1：Normal
	D[6]	1	RW	RST_I2C_MUX7_N 0：Reset I2C MUX7 1：Normal
	D[7]	1	RW	RST_I2C_MUX0_N 0：Reset I2C MUX0 1：Normal

BMC Reset				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x14	D[0]	1	RW	Reserved
	D[1]	1	RW	RST_BMC_PCIE_N/ RST_BMC_LPC_N 0：Reset BMC PCIE/LPC 1：Normal
	D[2]	1	RW	Reserved
	D[3]	1	RW	Reserved
	D[4]	1	RW	RST_BMC_WDT_L 0：Reset BMC watch dog 1：Normal
	D[5]	1	RW	Reserved
	D[6]	1	RW	Reserved
	D[7]	1	RW	Reserved

MAC &PHY Reset				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x15	D[0]	1	RW	RST_MAC_N 0：Reset MAC 1：Normal
	D[1]	1	RW	RST_PHY1_N 0：Reset PHY1 1：Normal
	D[2]	1	RW	Reserved
	D[3]	1	RW	Reserved
	D[4]	1	RW	Reserved
	D[5]	1	RW	Reserved
	D[6]	1	RW	Reserved
	D[7]	1	RW	Reserved

Miscellaneous Reset				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x16	D[0]	1	RW	RST_CJA_N 0：Reset clock buffer Si5344D 1：Normal
	D[1]	1	RW	RST_USB_BRIDGE_N 0：Reset USB bridge CP2130 1：Normal
	D[2]	1	RW	RST_SMU_N 0：Reset DPLL 82P33831 1：Normal
	D[3]	1	RW	Reserved
	D[4]	1	RW	RST_GNSS_N 0：Reset GNSS NEO-M8T 1：Normal
	D[5]	1	RW	RST_BITS_N 0：Reset BITS 82P2281 1：Normal
	D[6]	1	RW	RST_NIC1_N 0：Reset NIC1 I210 1：Normal
	D[7]	1	RW	RST_NIC1_PCIE_N 0：Reset NIC1 PCIE 1：Normal

Global Reset				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x17	D[0]	1	RW	Global reset 0：Reset Switch board 1：Normal
	D[1]	1	RW	Reserved
	D[2]	1	RW	Reserved
	D[3]	1	RW	Reserved
	D[4]	1	RW	Reserved
	D[5]	1	RW	Reserved
	D[6]	1	RW	Reserved
	D[7]	1	RW	Reserved

System LED Control1				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x18	D[0]	0	RW	SYNC Status LED On/Off 0：Off 1：On
	D[1]	0	RW	SYNC Status LED color 0：Yellow 1：Green
	D[2]	0	RW	GNSS Status LED On/Off 0：Off 1：On
	D[3]	0	RW	GNSS Status LED color 0：Yellow 1：Green
	D[4]	0	RW	Reserved
	D[5]	0	RW	Reserved
	D[6]	0	RW	System Status LED On/Off 0：Off 1：On
	D[7]	0	RW	System Status LED color 0：Yellow 1：Green

System LED Control2				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x19	D[0]	1	RW	Reserved
	D[1]	1	RW	Reserved
	D[2]	1	RW	Reserved

System LED Control2				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
	D[3]	1	RW	Reserved
	D[4]	1	RW	Reserved
	D[5]	1	RW	Reserved
	D[6]	1	RW	Reserved
	D[7]	1	RW	Reserved

System LED Blinking Control				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x1A	D[0]	0	RW	SYNC Status LED Blinking Status 0：Stable 1：Blinking
	D[1]	0	RW	GNSS Status LED Blinking Status 0：Stable 1：Blinking
	D[2]	0	RW	Reserved
	D[3]	0	RW	System Status LED Blinking Status 0：Stable 1：Blinking
	D[4]	0	RW	Reserved
	D[5]	0	RW	Reserved
	D[6]	0	RW	Reserved
	D[7]	0	RW	LED clear 0：Clear LED shift register 1：Normal

Fan4 & Fan5 TACH Switch				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x1B	D[0]	0	RW	Fan2 tach in control mode 0 ： CPLD output 1Khz PWM to control FAN45_TACH_SW 1：FAN45_TACH_SW is controlled by write register D[1]
	D[1]	0	RW	Fan2 tach in control 0: Reserved 1: FAN45_TACH_SW is connected to HWM_FAN4_TACH_IN
	D[2]	0	RW	Reserved
	D[3]	0	RW	Reserved
	D[4]	0	RW	Reserved
	D[5]	0	RW	Reserved
	D[6]	0	RW	Reserved
	D[7]	0	RW	Reserved

GNSS Status				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x1C	D[0]	1	RW	GNSS_ANT_SHORT_N 0：GNSS antenna is short 1：GNSS antenna is not short
	D[1]	0	RW	GNSS_ANT_OPEN_N 0：GNSS antenna is open 1：GNSS antenna is not open
	D[2]	0	RW	Reserved
	D[3]	0	RW	Reserved
	D[4]	0	RW	Reserved
	D[5]	0	RW	Reserved
	D[6]	0	RW	Reserved
	D[7]	0	RW	Reserved

Interrupt debug registor				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x1D	D[0]	1	RW	Debug Setting for Trigger INT_CHIP_CPLD_TO_CPU_N 0: Debug Trigger INT_CHIP_CPLD_TO_CPU_N 1: Normal
	D[1]	1	RW	Debug Setting for Trigger INT_CPLD_ALRM_N 0: Debug Trigger INT_CPLD_ALRM_N 1: Normal
	D[2]	1	RW	Debug Setting for Trigger I2C0_CPLD_ALRM_N 0: Debug Trigger I2C0_CPLD_ALRM_N 1: Normal
	D[3]	1	RW	Debug Setting for Trigger INT_CPLD_NMI_N 0: Debug Trigger Trigger INT_CPLD_NMI_N 1: Normal
	D[4]	1	RW	Debug Setting for Trigger INT_PTP_CPLD_TO_CPU_N 0: Debug Trigger INT_PTP_CPLD_TO_CPU_N 1: Normal
	D[5]	1	RW	Debug Setting for Trigger INT_SFP_CPLD_TO_CPU_N 0: Debug Trigger INT_SFP_CPLD_TO_CPU_N 1: Normal
	D[6]	1	RW	Reserved
	D[7]	1	RW	Reserved

TSPLL Clock Source Control				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x1E	D[1:0]	00	RW	JA_25M_SEL[1:0] 00: Config 0 01: Config 1 10: Config 2 11: Config 3
	D[2]	0	RW	Reserved
	D[3]	0	RW	Reserved
	D[4]	1	RW	JA_25M_CLKSEL 0: input clock source = DPLL3 for 8275.2 profile 1: input clock source = SyncE DPLL2 for 8275.1 profile

TSPLL Clock Source Control				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
	D[5]	0	RW	Reserved
	D[6]	0	RW	Reserved
	D[7]	0	RW	Reserved

5 Interrupt

5.1 Reset Control

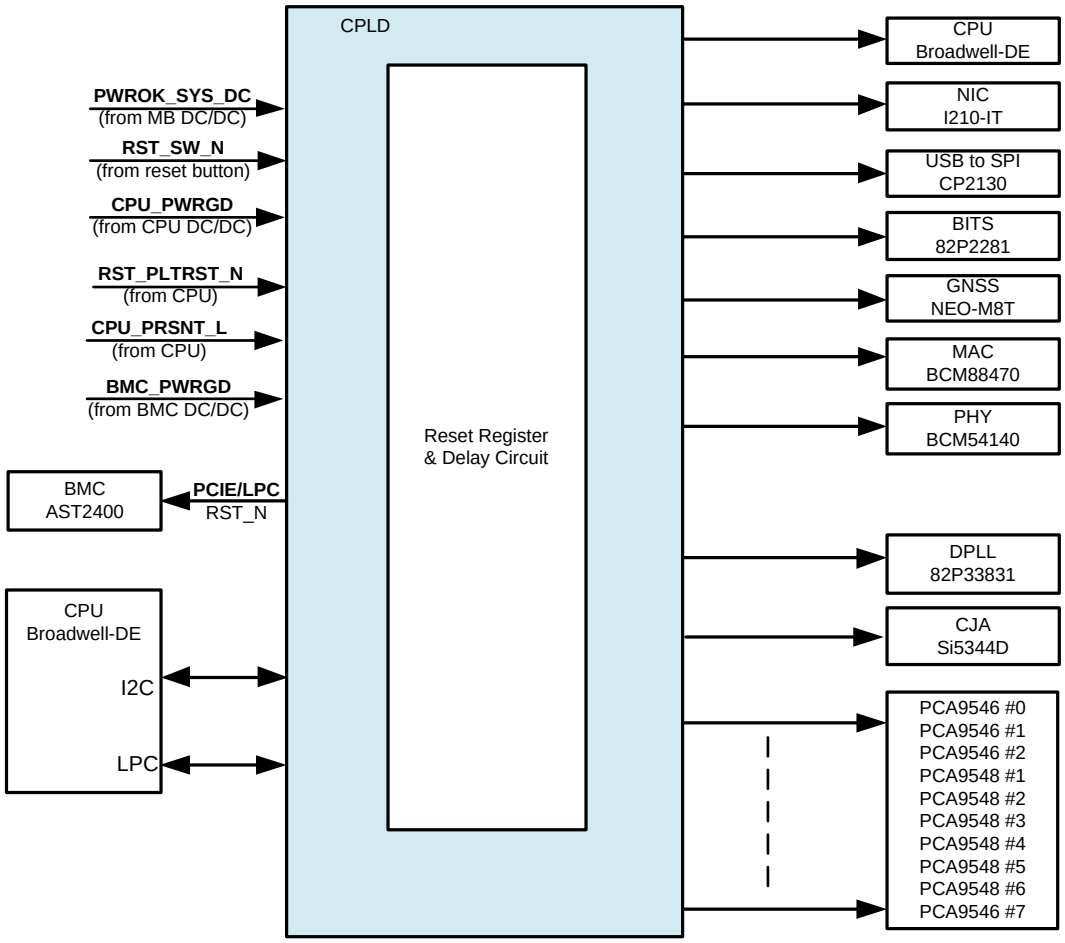


Figure 5-1 S9500-22XST System Reset Diagram

5.2 Hardware reset button

CPLD make the different reaction when the time to push reset button is different.

- Pushing button for less than 5s, CPLD will reset the whole system, except BMC.
- Pushing button for more than 5s, CPLD has no response.

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5.3 CPLD Interrupt Management

There are 5 interrupt signals to X86 CPU GPIO1, GPIO6, GPIO7, GPIO12, GPIO15 used for interrupt purpose, these GPIO pins should be configured as interrupt input and handle these events according to pre-defined priority. Any one of NMI, CHIP, PTP, SFP interrupts will generate an I2C alert event to CPU SMBus alert pin.

Receiving the 'Load Factory Default Interrupt', CPU should proceed system reboot and BIOS/ONIE/NOS images/pass words recovery to factory default.

'

5.3.1 Hardware Non-Maskable Interrupt

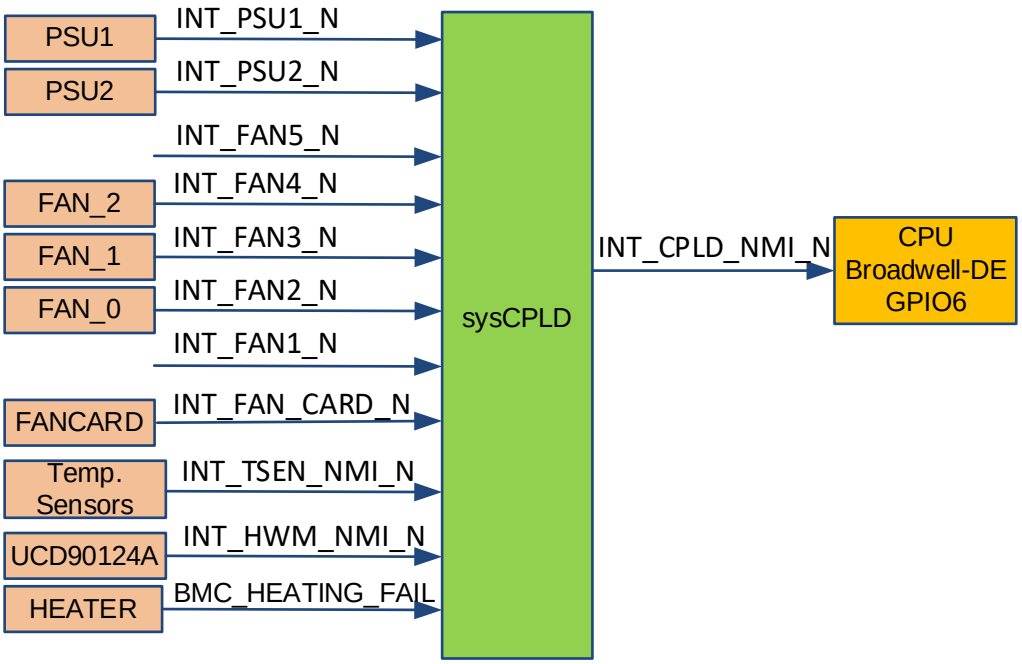


Figure 5-2 NMI Interrupt

5.3.2 Ethernet MAC/PHY Status Interrupt

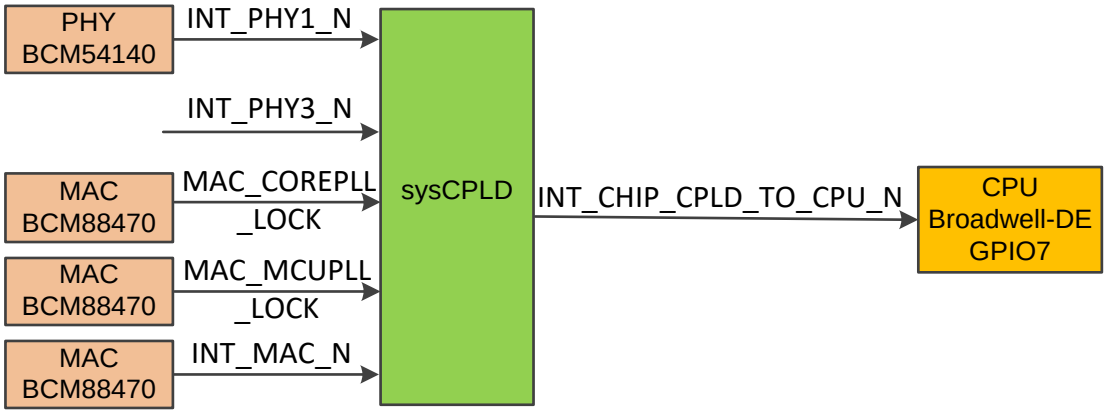


Figure 5-3 MAC &PHY Interrupt

5.3.3 SyncE and PTP Status Interrupt

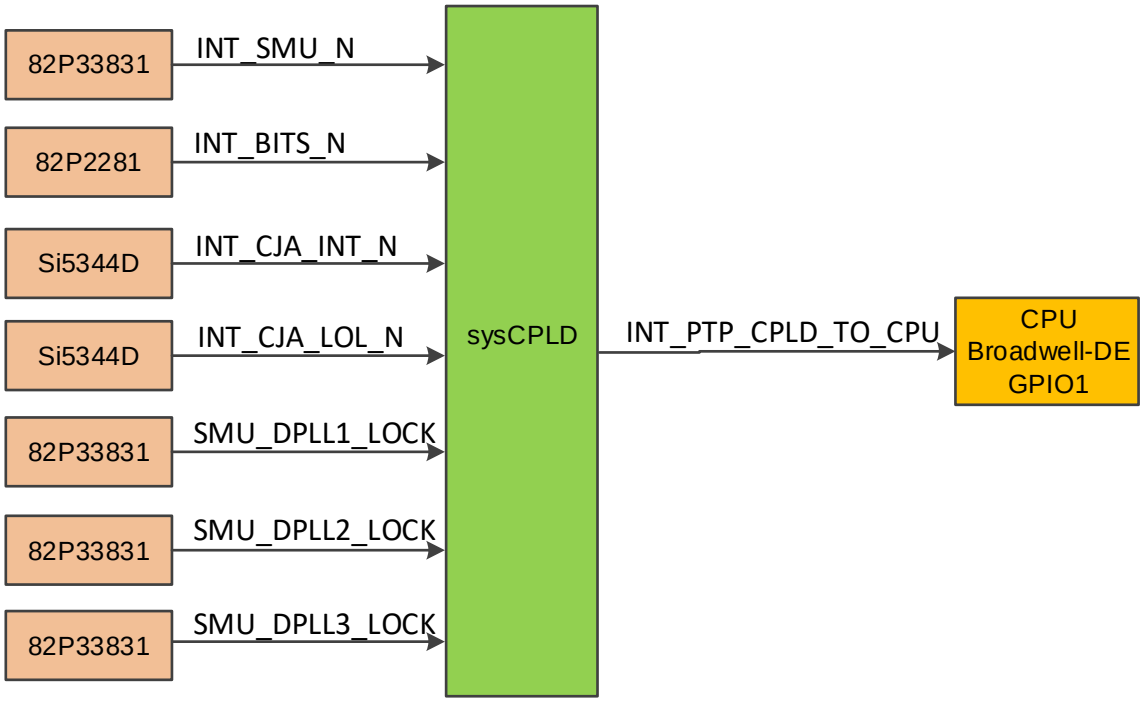


Figure 5-4 SyncE &PTP Interrupt

5.3.4 SFP+/SFP28/QSFP28 Port Status Interrupt

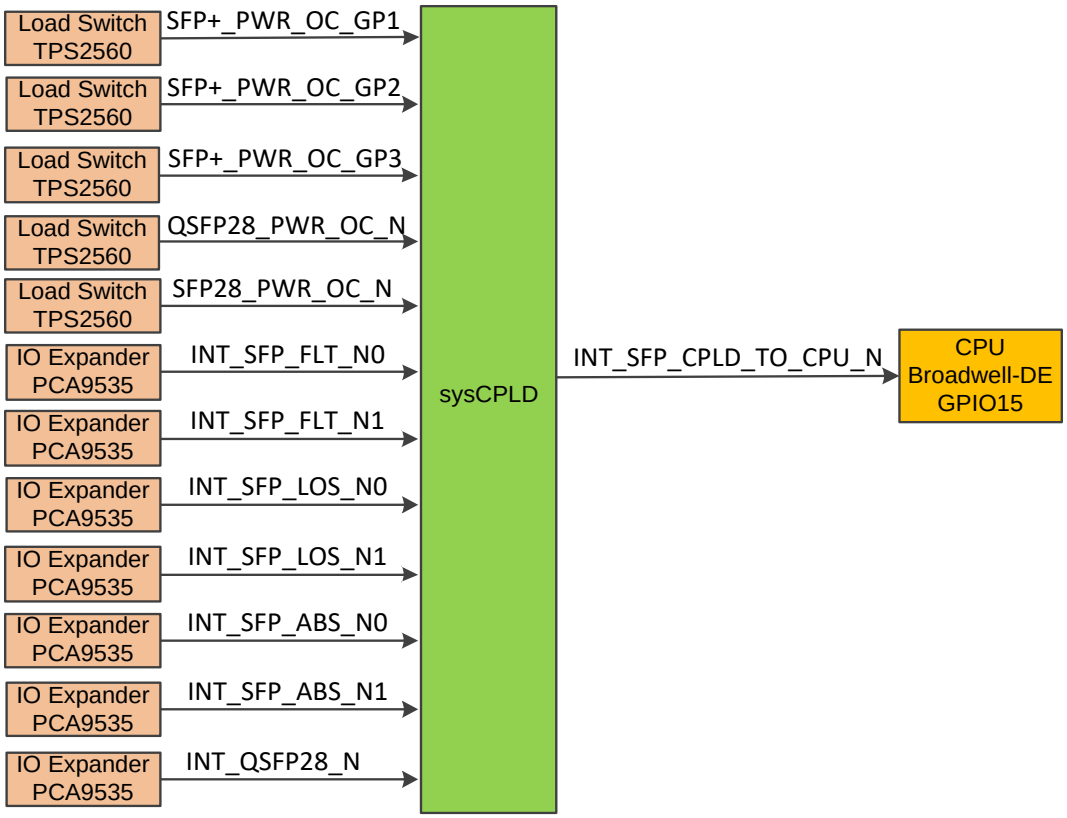


Figure 5-5 SFP+/SFP28/QSFP28 Interrupt

5.3.5 Load Factory Default Interrupt

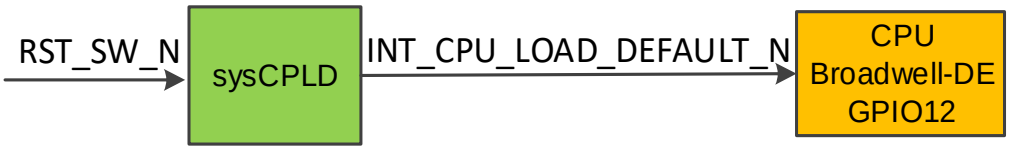


Figure 5-6 CPLD Alarm Interrupt

5.3.6 CPLD Alarm Interrupt

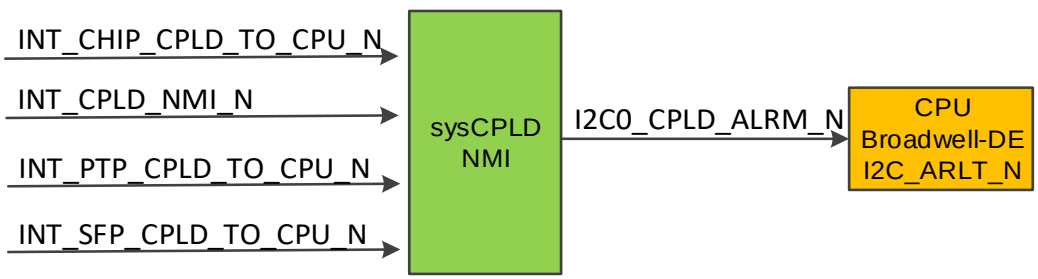


Figure 5-7 CPLD I2C Alarm Interrupt

6 LED

The front panel system status LED are placed on LED card. The bit stream of serial LED interface is shown as below:

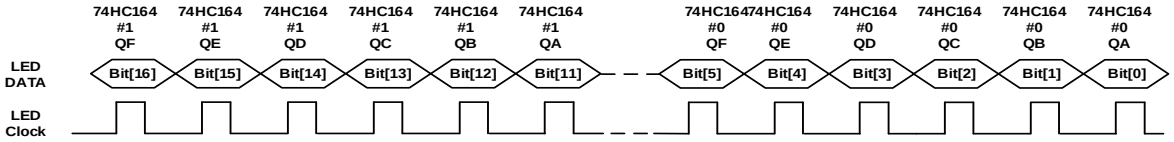


Figure 6-2 Bit stream of Front Panel LED interface

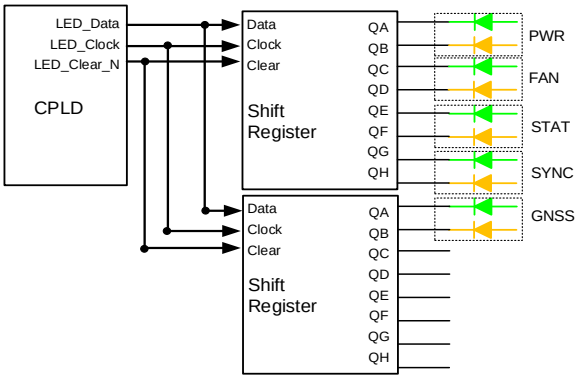


Figure 6-1 Front Panel LED Diagram

LED Function/State	Meaning	Comment
PWR (Green/Yellow): controlled by CPLD LED Interface Bit [0:1]		
OFF	No power or in shutdown mode.	Bit [0]=1; Bit [1]=1
Solid Green	System power good & BMC heating done	Bit [0]=0; Bit [1]=1
Blinking Green	System power good & BMC is heating	Bit [0]=0; Bit [1]=**B**
Solid Yellow	System power good but BMC heating fail	Bit [0]=1; Bit [1]=0
Blinking Yellow	System power fail	Bit [0]=**B**; Bit [1]=0
FAN (Green/Yellow): controlled by CPLD LED Interface Bit [2:3]		
OFF	Reserved	Bit [0]=1; Bit [1]=1
Solid Green	All FAN modules work well	Bit [0]=0; Bit [1]=1
Blinking Green	Reserved	Bit [0]=0; Bit [1]=**B**
Solid Yellow	Reserved	Bit [0]=1; Bit [1]=0
Blinking Yellow	One or more FAN module(s) fail or no FAN module present	Bit [0]=**B**; Bit [1]=0

STAT (Green/Yellow): controlled by CPLD LED Interface Bit [4:5]		
OFF	System (X86 & BMC) no boot	Bit [2]=1; Bit [3]=1
Solid Green	System boot complete **Note: need NOS to integrate this feature	Bit [2]=0; Bit [3]=1
Blinking Green	System is booting	Bit [2]=**B**; Bit [3]=1
Solid Yellow	Reserved	Bit [2]=1; Bit [3]=0
Blinking Yellow	Reserved	Bit [0]=**B**; Bit [1]=0
GNSS (Green/Yellow): controlled by CPLD LED Interface Bit [8:9]		
OFF	GNSS is not configured. **Note: need NOS to integrate this feature	Bit [8]=1; Bit [9]=1
Solid Green	GNSS is in normal state. Self-survey is complete. **Note: need NOS to integrate this feature	Bit [8]=0; Bit [9]=1
Blinking Green	GNSS is in learning state. Self-survey is not completed. **Note: need NOS to integrate this feature	Bit [8]= **B**; Bit [9]=1
Solid Yellow	Power up. GNSS is not tracking any satellite. **Note: need NOS to integrate this feature	Bit [8]=1; Bit [9]=0
Blinking Yellow	GNSS antenna is short to ground. **Note: need NOS to integrate this feature	Bit [8]= **B**; Bit [9]=1
SYNC (Green/Yellow): controlled by CPLD LED Interface Bit [10:11]		
OFF	System timing synchronization is disabled or in free-run mode. **Note: need NOS to integrate this feature	Bit [10]=1; Bit [11]=1
Solid Green	System timing core(1588 and SyncE) is synchronized to external timing source (ex: GNSS, 1PPS, PTP, BITS, etc) **Note: need NOS to integrate this feature	Bit [10]=0; Bit [11]=1
Blinking Green	System is synchronized in SyncE mode. **Note: need NOS to integrate this feature	Bit [10]= **B**; Bit [11]=1
Solid Yellow	System timing core is in acquiring state or holdover mode. **Note: need NOS to integrated this feature	Bit [10]=1; Bit [11]=0
Blinking Yellow	System timing synchronization fail. **Note: need NOS to integrated this feature	Bit [10]=1; Bit [11]= **B**
Note : **B**= Blinking, interleaved bit value with 1 and 0		